Microprocessor Architecture: From Simple Pipelines to Chip Multiprocessors

Jean-Loup Baer

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This book gives a comprehensive description of the architecture of microprocessors from simple in-order short pipeline designs to out-of-order superscalars. It discusses topics such as - the policies and mechanisms needed for out-of-order processing such as register renaming, reservation stations, and reorder buffers - optimizations for high performance such as branch predictors, instruction scheduling, and load-store speculations - design choices and enhancements to tolerate latency in the cache hierarchy of single and multiple processors - state-of-the-art multithreading and multiprocessing emphasizing single chip implementations Topics are presented as conceptual ideas, with metrics to assess the performance impact, if appropriate, and examples of realization. The emphasis is on how things work at a black box and algorithmic level. The author also provides sufficient detail at the register transfer level so that readers can appreciate how design features enhance performance as well as complexity.

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